Amendments to the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1-155. (Canceled)

156. (Previously Presented) A method of making an integrated circuit comprising:

providing a substrate having a principal surface;

forming circuit devices at least one of under and on the principal surface; and

forming a stress-controlled dielectric membrane overlying the circuit devices, wherein the stress-controlled dielectric membrane is capable of forming at least one of a flexible membrane, an elastic membrane, and a free standing membrane.

157. (Previously Presented) The method of claim 156, wherein the stress-controlled dielectric membrane comprises at least one or more stress-controlled dielectric layers.

158. (Previously Presented) The method of claim 157, wherein the at least one or more stress-controlled dielectric layers are caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the at least one or more stress-controlled dielectric layers.

159. (Previously Presented) The method of claim 158, wherein said stress is tensile.

160. (Previously Presented) The method of claim 157, comprising forming at least one of the at least one stress-controlled dielectric layers by depositing one or more stress-controlled dielectric films.

161. (Previously Presented) The method of claim 160, comprising depositing at least one of the one or more of the stress-controlled dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

162. (Previously Presented) The method of claim 156, wherein the stress-controlled dielectric membrane is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric membrane.

163. (Previously Presented) The method of claim 162, wherein said stress is tensile.

164. (Previously Presented) The method of claim 156, wherein said substrate is at least one of a semiconductor substrate, a silicon wafer, and a dielectric substrate.

165. (Previously Presented) The method of claim 156, wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

166. (Previously Presented) The method of claim 156, wherein the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

167. (Previously Presented) The method of claim 156, further comprising removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

168. (Previously Presented) The method of claim 167, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

169. (Previously Presented) A method of making an integrated circuit comprising:

providing a substrate having a principal surface;

forming sources, drains, and gates of circuit devices at least one of under and on the principal surface; and

forming a stress-controlled dielectric layer overlying selected ones of said sources, drains, and gates, wherein the stress-controlled dielectric layer is capable of forming at least one of a flexible membrane, an elastic membrane, and a free standing membrane.

170. (Previously Presented) The method of claim 169, wherein the stress-controlled dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

171. (Previously Presented) The method of claim 170, wherein said stress is tensile.

172. (Previously Presented) The method of claim 169, further comprising forming the stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

173. (Previously Presented) The method of claim 172, comprising depositing at least one of the one or more of the stress-controlled dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

174. (Previously Presented) The method of claim 169, wherein said substrate is at least one of a semiconductor substrate, a silicon wafer, and a dielectric substrate.

175. (Previously Presented) The method of claim 169, wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

176. (Previously Presented) The method of claim 169, wherein the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

177. (Previously Presented) The method of claim 169, further comprising removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

178. (Previously Presented) The method of claim 177, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

179. (Previously Presented) A method of making an integrated circuit comprising:

providing a substrate having a principal surface; and

forming circuitry at least one of under and on the principal surface of the substrate, said circuitry including a stress-controlled dielectric layer, one or more electrical interconnections, and a number of active devices, wherein the stress-controlled dielectric layer is capable of forming at least one of a flexible membrane, an elastic membrane, and a free standing membrane.

180. (Previously Presented) The method of claim 179, wherein the stress-controlled dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

181. (Previously Presented) The method of claim 180, wherein said stress is tensile.

182. (Previously Presented) The method of claim 179, further comprising forming the stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

183. (Previously Presented) The method of claim 182, comprising depositing at least one of the one or more of the stress-controlled dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

184. (Previously Presented) The method of claim 179, wherein said substrate is at least one of a semiconductor substrate, a silicon wafer, and a dielectric substrate.

185. (Previously Presented) The method of claim 179, wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

186. (Previously Presented) The method of claim 179, wherein the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

187. (Previously Presented) The method of claim 179, further comprising removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

188. (Previously Presented) The method of claim 187, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

189. (Previously Presented) A method of using an integrated circuit having a stress-controlled dielectric layer and interconnections formed passing through the stress-controlled dielectric layer, the method comprising:

transferring information through the stress-controlled dielectric layer by way of said interconnections, wherein the stress-controlled dielectric layer is capable of forming at least one of a flexible membrane, an elastic membrane, and a free standing membrane.

190. (Previously Presented) The method of claim 189, wherein the stress-controlled dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

191. (Previously Presented) The method of claim 190, wherein said stress is tensile.

192. (Previously Presented) The method of claim 189, further comprising forming the stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

193. (Previously Presented) The method of claim 192, comprising depositing at least one of the one or more of the

stress-controlled dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

194. (Currently Amended) The method of claim 189, further comprising a substrate, wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

195. (Currently Amended) The method of claim [[194]] 189, wherein the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

196. (Currently Amended) The method of claim 189, further comprising a substrate and removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

197. (Previously Presented) The method of claim 196, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

198. (Previously Presented) A method of using an integrated circuit having a data source formed on a first portion of the integrated circuit, a data sink formed on a second portion of the integrated circuit, and interconnect circuitry connecting the data source and the data sink, a

portion of the interconnect circuitry formed within a stress-controlled dielectric layer, the method comprising:

transferring data bytes between the data source and the data sink on the interconnect circuitry, wherein the stress-controlled dielectric layer is capable of forming at least one of a flexible membrane, an elastic membrane, and a free standing membrane.

199. (Previously Presented) The method of claim 198, wherein the stress-controlled dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

200. (Previously Presented) The method of claim 199, wherein said stress is tensile.

201. (Previously Presented) The method of claim 198, further comprising forming the stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

202. (Previously Presented) The method of claim 201, comprising depositing at least one of the one or more of the stress-controlled dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

203. (Currently Amended) The method of claim 198, <u>further comprising a substrate,</u> wherein the integrated circuit

is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

204. (Previously Presented) The method of claim 198, wherein the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity.

205. (Currently Amended) The method of claim 198, further comprising a substrate and removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

206. (Previously Presented) The method of claim 205, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

207. (Previously Presented) The method of claim 156, further comprising:

providing a second integrated circuit overlying the integrated circuit; and

providing an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

208. (Previously Presented) The method of claim 156, further comprising:

providing a plurality of integrated circuits overlying the integrated circuit; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit.

209. (Previously Presented) The method of claim 179, further comprising:

providing a second integrated circuit overlying the integrated circuit; and

providing an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

210. (Previously Presented) The method of claim 179, further comprising:

providing a plurality of integrated circuits overlying the integrated circuit; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit.

211. (Previously Presented) The method of claim 189, further comprising:

providing a second integrated circuit overlying the integrated circuit; and

providing an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

212. (Previously Presented) The method of claim 189, further comprising:

providing a plurality of integrated circuits overlying the integrated circuit; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit.

213. (Previously Presented) The method of claim 198, further comprising:

a second integrated circuit overlying the integrated circuit; and

interconnect connecting portions of the circuitry of the second integrated circuit and the integrated circuit.

214. (Previously Presented) The method of claim 198, further comprising:

providing a plurality of integrated circuits overlying the integrated circuit; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit.

215. (Currently Amended) The method of claim 157, wherein the at least one or more stress-controlled dielectric layers are caused to have at least one of a tensile stress and a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

216. (Currently Amended) The method of claim 169, wherein the stress-controlled dielectric layer is caused to have

at least one of a tensile stress and a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

217. (Currently Amended) The method of claim 179, wherein the stress-controlled dielectric layer is caused to have at least one of a tensile stress and a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

218. (Currently Amended) The method of claim 189, wherein the stress-controlled dielectric layer is caused to have at least one of a tensile stress and a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

219. (Currently Amended) The method of claim 198, wherein the stress-controlled dielectric layer are caused to have at least one of a tensile stress and a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

220. (Previously Presented) A method of making an integrated circuit comprising:

forming circuitry having active devices at least one of in and on a substrate; and

forming a stress-controlled dielectric membrane as part of said circuitry;

wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

221. (Previously Presented) The method of claim 220, wherein the integrated circuit is able to be thinned to about 50 microns or less while retaining its structural integrity.

222. (Previously Presented) The method of claim 220, wherein said substrate is at least one of a semiconductor substrate, a silicon wafer, and a dielectric substrate.

223. (Previously Presented) The method of claim 220, further comprising removing a major portion of the substrate.

224. (Previously Presented) The method of claim 223, wherein the major portion of the substrate is removed prior to forming said circuitry.

225. (Previously Presented) The method of claim 223, wherein the major portion of the substrate is removed after forming said circuitry.

226. (Previously Presented) The method of claim 220, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

227. (Previously Presented) The method of claim 220, wherein the stress-controlled dielectric membrane is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less

and 2 to 100 times less than the fracture strength of the stress-controlled dielectric membrane.

228. (Previously Presented) The method of claim 227, wherein said stress is tensile.

229. (Previously Presented) The method of claim 220, wherein the stress-controlled dielectric membrane comprises at least one or more stress-controlled dielectric layers.

230. (Previously Presented) The method of claim 220, wherein the major portion of the substrate is removed prior to forming said circuitry.

231. (Previously Presented) The method of claim 220, wherein the major portion of the substrate is removed after forming said circuitry.

232. (Previously Presented) The method of claim 220, comprising forming the stress-controlled dielectric membrane by deposition of one or more stress-controlled dielectric films.

233. (Previously Presented) The method of claim 232, comprising depositing at least one of the one or more of the stress-controlled dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

234. (Previously Presented) A method of making an integrated circuit comprising:

forming circuitry having active devices at least one of in and on a substrate; and

forming a stress-controlled dielectric layer as part of said circuitry;

wherein the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity.

235. (Previously Presented) The method of claim 234, wherein the integrated circuit is able to be thinned to about 50 microns or less while retaining its structural integrity.

236. (Previously Presented) The method of claim 234, comprising forming the stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

237. (Previously Presented) The method of claim 236, comprising depositing at least one of the one or more of the stress-controlled dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

238. (Previously Presented) The method of claim 234, wherein said substrate is at least one of a semiconductor substrate, a silicon wafer, and a dielectric substrate.

239. (Previously Presented) The method of claim 234, further comprising removing a major portion of the substrate.

240. (Previously Presented) The method of claim 239, wherein the major portion of the substrate is removed prior to forming said circuitry.

241. (Previously Presented) The method of claim 239, wherein the major portion of the substrate is removed after forming said circuitry.

242. (Previously Presented) The method of claim 234, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

243. (Previously Presented) The method of claim 234, wherein the stress-controlled dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

244. (Previously Presented) The method of claim 243, wherein said stress is tensile.

245. (Previously Presented) A method of making an integrated circuit comprising:

forming circuitry having active devices at least one of in and on a substrate; and

forming a stress-controlled dielectric layer as part of said circuitry; and

removing a major portion of the substrate throughout a full extent thereof without impairing the structural integrity of the integrated circuit.

246. (Previously Presented) The method of claim 245, wherein the major portion of the substrate is removed prior to forming said circuitry.

247. (Previously Presented) The method of claim 245, wherein the major portion of the substrate is removed after forming said circuitry.

248. (Previously Presented) The method of claim 245, comprising forming the stress-controlled dielectric layer by deposition of one or more stress-controlled dielectric films.

249. (Previously Presented) The method of claim 248, comprising depositing at least one of the one or more of the stress-controlled dielectric films using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

250. (Previously Presented) The method of claim 245, wherein said substrate is at least one of a semiconductor substrate, a silicon wafer, and a dielectric substrate.

251. (Previously Presented) The method of claim 156, wherein the major portion of the substrate is removed prior to forming said circuitry.

252. (Previously Presented) The method of claim 156, wherein the major portion of the substrate is removed after forming said circuitry.

253. (Previously Presented) The method of claim 245, wherein the integrated circuit is caused to have a thickness of about 50 microns or less.

254. (Previously Presented) The method of claim 245, wherein the stress-controlled dielectric layer is caused to have a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

255. (Previously Presented) The method of claim 254, wherein said stress is tensile.

256. (Previously Presented) The method of claim 220, further comprising:

forming a second integrated circuit overlying the integrated circuit; and

forming an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

257. (Previously Presented) The method of claim 220, further comprising:

forming a plurality of integrated circuits overlying the integrated circuit; and

forming at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuit and the integrated circuit.

258. (Previously Presented) The method of claim 234, further comprising:

forming a second integrated circuit overlying the integrated circuit; and

forming an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

259. (Previously Presented) The method of claim 234, further comprising:

forming a plurality of integrated circuits overlying the integrated circuit; and

forming at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuit and the integrated circuit.

260. (Previously Presented) The method of claim 245, further comprising:

forming a second integrated circuit overlying the integrated circuit; and

forming an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

261. (Previously Presented) The method of claim 245, further comprising:

forming a plurality of integrated circuits overlying the integrated circuit; and

forming at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuit and the integrated circuit.

262. (Currently Amended) The method of claim 229, wherein the at least one or more stress-controlled dielectric layers are caused to have at least one of a tensile stress and a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

263. (Currently Amended) The method of claim 234, wherein the stress-controlled dielectric layer is caused to have at least one of a tensile stress and a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

264. (Currently Amended) The method of claim 245, wherein the stress-controlled dielectric layer is caused to have at least one of a tensile stress and a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

265. (Previously Presented) The method of claim 169, further comprising:

providing a second integrated circuit overlying the integrated circuit; and

providing an interconnect that connects portions of the circuitry of the second integrated circuit and the integrated circuit.

266. (Previously Presented) The method of claim 169, further comprising:

providing a plurality of integrated circuits overlying the integrated circuit; and

providing at least one interconnect that connects portions of the circuitry of at least one of the plurality of integrated circuits and the integrated circuit.

267. (Currently Amended) The method of claim 229, wherein the at least one or more stress-controlled dielectric layers are caused to have at least one of a tensile stress and a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the at least one or more stress-controlled dielectric layers.

268. (Previously Presented) The method of claim 229, wherein the at least one or more stress-controlled dielectric layers are caused to be at least one of elastic and substantially flexible.

269. (Currently Amended) The method of claim 229, wherein the at least one or more stress-controlled dielectric layers are caused to be at least one of elastic and substantially flexible and the at least one or more stress-controlled dielectric layers are caused to have at least one of a tensile stress and a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the at least one or more stress-controlled dielectric layers.

270. (Currently Amended) The method of claim 229, wherein the at least one or more stress-controlled dielectric layers are caused to be at least one of elastic and substantially flexible and the at least one or more stress-controlled dielectric layers are caused to have at least one of a tensile stress and a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

271. (Previously Presented) The method of claim 157, wherein the at least one or more stress-controlled dielectric layers are caused to be at least one of elastic and substantially flexible.

272. (Currently Amended) The method of claim 157, wherein the at least one or more stress-controlled dielectric layers are caused to have at least one of a tensile stress and a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the at least one or more stress-controlled dielectric layers.

273. (Currently Amended) The method of claim 157, wherein the at least one or more stress-controlled dielectric layers are caused to be at least one of elastic and substantially flexible and the at least one or more stress-controlled dielectric layers are caused to have at least one of a tensile stress and a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

274. (Previously Presented) The method of claim 169, wherein the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible.

275. (Currently Amended) The method of claim 169, wherein the stress-controlled dielectric layer is caused to have at least one of a tensile stress and a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

276. (Currently Amended) The method of claim 169, wherein the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible and the stress-controlled dielectric layer is caused to have at least one of a tensile stress and a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

277. (Previously Presented) The method of claim 179, wherein the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible.

278. (Currently Amended) The method of claim 179, wherein the stress-controlled dielectric layer is caused to have at least one of a tensile stress and a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

279. (Currently Amended) The method of claim 179, wherein the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible and the stress-controlled dielectric layer is caused to have at least one of a tensile stress and a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

280. (Previously Presented) The method of claim 189, wherein the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible.

281. (Currently Amended) The method of claim 189, wherein the stress-controlled dielectric layer is caused to have at least one of a tensile stress and a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

282. (Currently Amended) The method of claim 189, wherein the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible and the stress-controlled dielectric layer is caused to have at least one of a tensile stress and a stress of about 8×10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

283. (Previously Presented) The method of claim 198, wherein the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible.

284. (Currently Amended) The method of claim 198, wherein the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible and the stress-controlled dielectric layer is caused to have at least one of a tensile stress and a stress of at least one of about 8 x 10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

285. (Currently Amended) The method of claim 198, wherein the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible and the stress-controlled dielectric layer is caused to have at least one of a tensile stress and a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

286. (Previously Presented) The method of claim 234, wherein the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible.

287. (Currently Amended) The method of claim 234, wherein the stress-controlled dielectric layer is caused to have at least one of a tensile stress and a stress of at least one of about 8 x 10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

288. (Currently Amended) The method of claim 234, wherein the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible and the stress-controlled dielectric layer is caused to have at least

one of a tensile stress and a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

289. (Previously Presented) The method of claim 245, wherein the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible.

290. (Currently Amended) The method of claim 245, wherein the stress-controlled dielectric layer is caused to have at least one of a tensile stress and a stress of at least one of about 8 x 10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer.

291. (Currently Amended) The method of claim 245, wherein stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible and the stress-controlled dielectric layer is caused to have at least one of a tensile stress and a stress of about 8 x 10^8 dynes/cm^2 or less and the integrated circuit is caused to have a thickness of about 50 microns or less.

292-393. (Canceled)

394. (Previously Presented) The method of claim 156, further comprising forming a barrier layer in the substrate parallel to the principal surface before forming the circuit devices, the principal surface overlying the barrier layer.

395. (Previously Presented) The method of claim 169, further comprising forming a barrier layer in the substrate parallel to the principal surface before forming the circuit devices, the principal surface overlying the barrier layer.

396. (Previously Presented) The method of claim 179, further comprising forming a barrier layer in the substrate parallel to the principal surface before forming the circuitry, the principal surface overlying the barrier layer.

397. (Previously Presented) The method of claim 220, further comprising:

providing a principal surface on the substrate; and

forming a barrier layer in the substrate parallel to the principal surface before forming the circuitry having active devices, the principal surface overlying the barrier layer.

398. (Previously Presented) The method of claim 234, further comprising: providing a principal surface on the substrate; and
forming a barrier layer in the substrate parallel to the principal surface before forming the circuitry having active devices, the principal surface overlying the barrier layer.

399. (Previously Presented) The method of claim 245, further comprising:

providing a principal surface on the substrate; and

forming a barrier layer in the substrate parallel to the principal surface before forming the circuitry having active devices, the principal surface overlying the barrier layer.

400-408. (Canceled)

409. (Currently Amended) The method of claim 157, wherein the at least one or more stress-controlled dielectric layers are formed from at least one of an inorganic dielectric material and an organic dielectric material.

410. (Previously Presented) The method of claim 409, wherein at least a major portion of the inorganic dielectric material is formed from at least one of an oxide of silicon and a nitride of silicon.

411. (Previously Presented) The method of claim 169, wherein the stress-controlled dielectric layer is formed from at least one of an inorganic dielectric material and an organic dielectric material.

412. (Previously Presented) The method of claim 411, wherein at least a major portion of the inorganic dielectric material is formed from at least one of an oxide of silicon and a nitride of silicon.

413. (Previously Presented) The method of claim 179, wherein the stress-controlled dielectric layer is formed from at

least one of an inorganic dielectric material and an organic dielectric material.

414. (Previously Presented) The method of claim 413, wherein at least a major portion of the inorganic dielectric material is formed from at least one of an oxide of silicon and a nitride of silicon.

415. (Previously Presented) The method of claim 189, wherein the stress-controlled dielectric layer is formed from at least one of an inorganic dielectric material and an organic dielectric material.

416. (Previously Presented) The method of claim 415, wherein at least a major portion of the inorganic dielectric material is formed from at least one of an oxide of silicon and a nitride of silicon.

417. (Previously Presented) The method of claim 198, wherein the stress-controlled dielectric layer is formed from at least one of an inorganic dielectric material and an organic dielectric material.

418. (Previously Presented) The method of claim 417, wherein at least a major portion of the inorganic dielectric material is formed from at least one of an oxide of silicon and a nitride of silicon.

419. (Previously Presented) The method of claim 220, wherein the stress-controlled dielectric membrane is formed from

at least one of an inorganic dielectric material and an organic dielectric material.

420. (Previously Presented) The method of claim 419, wherein at least a major portion of the inorganic dielectric material is formed from at least one of an oxide of silicon and a nitride of silicon.

421. (Previously Presented) The method of claim 234, wherein the stress-controlled dielectric layer is formed from at least one of an inorganic dielectric material and an organic dielectric material.

422. (Previously Presented) The method of claim 421, wherein at least a major portion of the inorganic dielectric material is formed from at least one of an oxide of silicon and a nitride of silicon.

423. (Previously Presented) The method of claim 245, wherein the stress-controlled dielectric layer is formed from at least one of an inorganic dielectric material and an organic dielectric material.

424. (Previously Presented) The method of claim 423, wherein at least a major portion of the inorganic dielectric material is formed from at least one of an oxide of silicon and a nitride of silicon.

425-447. (Canceled)

448. (Currently Amended) The method of claim 157, further comprising a plurality of interconnect conductors formed ~~within~~ as part of at least one of the at least one or more stress-controlled dielectric layers, wherein the interconnect conductors are at least one of electrical and optical interconnect conductors.

449. (Previously Presented) The method of claim 156, further comprising at least one flexible integrated circuit overlying the integrated circuit.

450. (Previously Presented) The method of claim 156, wherein the integrated circuit is capable of forming at least one of a substantially flexible integrated circuit and an elastic integrated circuit.

451. (Previously Presented) The method of claim 157, wherein at least one of the at least one or more stress-controlled dielectric layers is capable of forming at least one of a flexible membrane, an elastic membrane and a free standing membrane.

452. (Previously Presented) The method of claim 157, wherein at least one of the at least one or more stress-controlled dielectric layers is formed at a temperature of about 400°C.

453. (Currently Amended) The method of claim 169, further comprising a plurality of interconnect conductors formed ~~within~~ as part of the stress-controlled dielectric layer,

wherein the interconnect conductors are at least one of electrical and optical interconnect conductors.

454. (Previously Presented) The method of claim 169, further comprising at least one flexible integrated circuit overlying the integrated circuit.

455. (Previously Presented) The method of claim 169, wherein the integrated circuit is capable of forming at least one of a substantially flexible integrated circuit and an elastic integrated circuit.

456. (Canceled)

457. (Previously Presented) The method of claim 169, wherein the stress-controlled dielectric layer is formed at a temperature of about 400°C.

458. (Currently Amended) The method of claim 179, further comprising a plurality of interconnect conductors formed ~~within~~ as part of the stress-controlled dielectric layer, wherein the interconnect conductors are at least one of electrical and optical interconnect conductors.

459. (Previously Presented) The method of claim 179, further comprising at least one flexible integrated circuit overlying the integrated circuit.

460. (Previously Presented) The method of claim 179, wherein the integrated circuit is capable of forming at least

one of a substantially flexible integrated circuit and an elastic integrated circuit.

461. (Canceled)

462. (Previously Presented) The method of claim 179, wherein the stress-controlled dielectric layer is formed at a temperature of about 400°C.

463. (Previously Presented) The method of claim 189, further comprising at least one flexible integrated circuit overlying the integrated circuit.

464. (Previously Presented) The method of claim 189, wherein the integrated circuit is capable of forming at least one of a substantially flexible integrated circuit and an elastic integrated circuit.

465. (Canceled)

466. (Previously Presented) The method of claim 189, wherein the stress-controlled dielectric layer is caused to have a withstand temperature of about 400°C or less.

467. (Previously Presented) The method of claim 198, further comprising at least one flexible integrated circuit overlying the integrated circuit.

468. (Previously Presented) The method of claim 198, wherein the integrated circuit is capable of forming at least

one of a substantially flexible integrated circuit and an elastic integrated circuit.

469. (Canceled)

470. (Previously Presented) The method of claim 198, wherein the stress-controlled dielectric layer is formed at a temperature of about 400°C.

471. (Currently Amended) The method of claim 229, further comprising a plurality of interconnect conductors formed ~~within~~ as part of at least one of the at least one or more stress-controlled dielectric layers, wherein the interconnect conductors are at least one of electrical and optical interconnect conductors.

472. (Previously Presented) The method of claim 220, further comprising at least one flexible integrated circuit overlying the integrated circuit.

473. (Previously Presented) The method of claim 220, wherein the integrated circuit is capable of forming at least one of a substantially flexible integrated circuit and an elastic integrated circuit.

474. (Previously Presented) The method of claim 229, wherein the at least one or more stress-controlled dielectric layers are capable of forming at least one of a flexible membrane, an elastic membrane and a free standing membrane.

475. (Previously Presented) The method of claim 229, wherein the at least one or more stress-controlled dielectric layers are formed at a temperature of about 400°C.

476. (Currently Amended) The method of claim 234, further comprising a plurality of interconnect conductors formed ~~within~~ as part of the stress-controlled dielectric layer, wherein the interconnect conductors are at least one of electrical and optical interconnect conductors.

477. (Previously Presented) The method of claim 234, further comprising at least one flexible integrated circuit overlying the integrated circuit.

478. (Previously Presented) The method of claim 234, wherein the integrated circuit is capable of forming at least one of a substantially flexible integrated circuit and an elastic integrated circuit.

479. (Previously Presented) The method of claim 234, wherein the stress-controlled dielectric layer is capable of forming at least one of a flexible membrane, an elastic membrane and a free standing membrane.

480. (Previously Presented) The method of claim 234, wherein the stress-controlled dielectric layer is formed at a temperature of about 400°C.

481. (Currently Amended) The method of claim 245, further comprising a plurality of interconnect conductors formed

~~within~~ as part of the stress-controlled dielectric layer, wherein the interconnect conductors are at least one of electrical and optical interconnect conductors.

482. (Previously Presented) The method of claim 245, further comprising at least one flexible integrated circuit overlying the integrated circuit.

483. (Previously Presented) The method of claim 245, wherein the integrated circuit is capable of forming at least one of a substantially flexible integrated circuit and an elastic integrated circuit.

484. (Previously Presented) The method of claim 245, wherein the stress-controlled dielectric layer is capable of forming at least one of a flexible membrane, an elastic membrane and a free standing membrane.

485. (Previously Presented) The method of claim 245, wherein the stress-controlled dielectric layer is formed at a temperature of about 400°C.

486-522. (Canceled)

523. (New) The method of claim 157, wherein at least one of said substrate is at least one of a semiconductor substrate, a silicon wafer, and a dielectric substrate, the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity, the integrated circuit is

able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity, the integrated circuit is caused to have a thickness of about 50 microns or less, the at least one or more stress-controlled dielectric layers are caused to have at least one of a tensile stress and a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the at least one or more stress-controlled dielectric layers, at least one of the at least one or more stress-controlled dielectric layers is caused to be at least one of elastic and substantially flexible, at least one of the at least one or more stress-controlled dielectric layers is capable of forming a free standing membrane, at least one of the at least one or more stress-controlled dielectric layers is formed from at least one of an inorganic dielectric material and an organic dielectric material with at least a major portion of the inorganic dielectric material formed from at least one of an oxide of silicon and a nitride of silicon, at least one of the at least one or more stress-controlled dielectric layers is formed with at least one of electrical and optical interconnect conductors, and at least one of the at least one or more stress-controlled dielectric layers is deposited using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

524. (New) The method of claim 169, wherein at least one of said substrate is at least one of a semiconductor substrate, a silicon wafer, and a dielectric substrate, the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while

retaining its structural integrity, the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity, the integrated circuit is caused to have a thickness of about 50 microns or less, the stress-controlled dielectric layer is caused to have at least one of a tensile stress and a stress of at least one of about 8 x 10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer, the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible, the stress-controlled dielectric layer is formed from at least one of an inorganic dielectric material and an organic dielectric material with at least a major portion of the inorganic dielectric material formed from at least one of an oxide of silicon and a nitride of silicon, the stress-controlled dielectric layer is formed with at least one of electrical and optical interconnect conductors, and the stress-controlled dielectric layer is deposited using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

525. (New) The method of claim 179, wherein at least one of said substrate is at least one of a semiconductor substrate, a silicon wafer, and a dielectric substrate, the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity, the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity, the integrated circuit is caused to have a thickness of about 50

microns or less, the stress-controlled dielectric layer is caused to have at least one of a tensile stress and a stress of at least one of about 8 x 10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer, the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible, the stress-controlled dielectric layer is formed from at least one of an inorganic dielectric material and an organic dielectric material with at least a major portion of the inorganic dielectric material formed from at least one of an oxide of silicon and a nitride of silicon, the stress-controlled dielectric layer is formed with at least one of electrical and optical interconnect conductors, and the stress-controlled dielectric layer is deposited using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

526. (New) The method of claim 189, wherein at least one of the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity, the integrated circuit is caused to have a thickness of about 50 microns or less, the stress-controlled dielectric layer is caused to have at least one of a tensile stress and a stress of at least one of about 8 x 10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer, the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible, the stress-controlled dielectric layer is formed from at least one of an inorganic dielectric material and an organic dielectric material with at

least a major portion of the inorganic dielectric material formed from at least one of an oxide of silicon and a nitride of silicon, the stress-controlled dielectric layer is formed with at least one of electrical and optical interconnect conductors, and the stress-controlled dielectric layer is deposited using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

527. (New) The method of claim 198, wherein at least one of the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity, the integrated circuit is caused to have a thickness of about 50 microns or less, the stress-controlled dielectric layer is caused to have at least one of a tensile stress and a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer, the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible, the stress-controlled dielectric layer is formed from at least one of an inorganic dielectric material and an organic dielectric material with at least a major portion of the inorganic dielectric material formed from at least one of an oxide of silicon and a nitride of silicon, the stress-controlled dielectric layer is formed with at least one of electrical and optical interconnect conductors, and the stress-controlled dielectric layer is deposited using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

528. (New) The method of claim 229, wherein at least one of said substrate is at least one of a semiconductor substrate, a silicon wafer, and a dielectric substrate, the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity, the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity, the integrated circuit is caused to have a thickness of about 50 microns or less, the at least one or more stress-controlled dielectric layers are caused to have at least one of a tensile stress and a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the at least one or more stress-controlled dielectric layers, at least one of the at least one or more stress-controlled dielectric layers is caused to be at least one of elastic and substantially flexible, at least one of the at least one or more stress-controlled dielectric layers is capable of forming a free standing membrane, at least one of the at least one or more stress-controlled dielectric layers is formed from at least one of an inorganic dielectric material and an organic dielectric material with at least a major portion of the inorganic dielectric material formed from at least one of an oxide of silicon and a nitride of silicon, at least one of the at least one or more stress-controlled dielectric layers is formed with at least one of electrical and optical interconnect conductors, and at least one of the at least one or more stress-controlled dielectric layers is deposited using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

529. (New) The method of claim 234, wherein at least one of the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity, the integrated circuit is able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity, the integrated circuit is caused to have a thickness of about 50 microns or less, the stress-controlled dielectric layer is caused to have at least one of a tensile stress and a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer, the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible, the stress-controlled dielectric layer is capable of forming a free standing membrane, the stress-controlled dielectric layer is formed from at least one of an inorganic dielectric material and an organic dielectric material with at least a major portion of the inorganic dielectric material formed from at least one of an oxide of silicon and a nitride of silicon, the stress-controlled dielectric layer is formed with at least one of electrical and optical interconnect conductors, and the stress-controlled dielectric layer is deposited using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.

530. (New) The method of claim 245, wherein at least one of the integrated circuit is able to have a major portion of the substrate removed throughout a full extent thereof while retaining its structural integrity, the integrated circuit is

able to be thinned to about 50 microns or less throughout a full extent thereof while retaining its structural integrity, the integrated circuit is caused to have a thickness of about 50 microns or less, the stress-controlled dielectric layer is caused to have at least one of a tensile stress and a stress of at least one of about 8×10^8 dynes/cm^2 or less and 2 to 100 times less than the fracture strength of the stress-controlled dielectric layer, the stress-controlled dielectric layer is caused to be at least one of elastic and substantially flexible, the stress-controlled dielectric layer is capable of forming a free standing membrane, the stress-controlled dielectric layer is formed from at least one of an inorganic dielectric material and an organic dielectric material with at least a major portion of the inorganic dielectric material formed from at least one of an oxide of silicon and a nitride of silicon, the stress-controlled dielectric layer is formed with at least one of electrical and optical interconnect conductors, and the stress-controlled dielectric layer is deposited using at least one of multiple RF energy sources, Chemical Vapor Deposition, and Plasma Enhanced Chemical Vapor Deposition.